Analysis and Design of SR Driver Circuit for LLC DC-DC Converter Under High Load Current Application

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***Abstract*—In low output voltage high load current LLC dc-dc converters, synchronous rectifiers are usually used to reduce the secondary loss. The proper conduction time of synchronous rectifiers (SRs) is key to improve efficiency and make the converter run more reliably and stably. In high load current LLC dc-dc converters, voltage ringing across SRs makes SRs turn-on early when the current flowing through SRs decreases to zero, which causes the circuit to work abnormally. This paper presents analysis and design of SR driver circuit for LLC dc-dc converter under high load current application and eliminates the effect of voltage ringing across SRs by a RC filter. The proposed filter is simple and lossless, which is easy to utilize in the circuit. The voltage ringing across SRs is analyzed and the design parameters of the filter are given in this paper. The experimental results show that 1.26kW LLC dc-dc converter with the proposed filter works reliably at high load current with high efficiency and high-power density.**

Keywords—LLC dc-dc converter, Synchronous rectifier, Driver circuit, High load current

I. INTRODUCTION

High efficiency and high power-density switching power supplies are increasingly required. For this reason, resonant dc-dc converters, such as LLC dc-dc converter, which have become more popular and is used widely in power supply application as this circuit benefits from simplicity, low cost, high efficiency and soft-switching. However, due to the forward voltage drop of rectifier diodes, there is significant loss on rectifier diodes in some low output voltage high load current applications. Therefore, synchronous rectifiers (SRs) are always utilized for high load current LLC dc-dc converters to reduce the secondary loss [1].

In high load current application, the loss of body diodes of SRs is much higher than conduction loss of SRs, thus the optimal efficiency of the converter depends on the well adjustment of SRs gate driving signals. SR driving strategies are mainly classified as current driven methods and v_{DS} of SR sensing methods. In [2]-[3], current transformers (CTs) are used to sense the primary current, and a current-compensating winding in current transformer (CT) is used to cancel out the magnetizing current and generate suitable driving signals for SR. However, the CTs are lossy and bulky, which is unsuitable to high efficiency and high power-density design. The v_{DS} of SR sensing methods save the current sensors by sensing the drain-source voltage across the SR MOSFET. Generally, when the voltage across SRs are detected to reach to forward drop voltage of body diodes $-V_F$ for several nanosecond continuously, SRs are turned on; and when the voltage across SRs are detected to reach to zero, SRs are turned off. However, if the SR is turned off too early, the loss of body diodes of SR is large, which reduces the efficiency of the circuit; if the SR is turned off too late, the current flowing through the secondary side SR backflow and cause energy transferring backward to primary side or even other disastrous situations. Therefore, it is important make SR turn-on and turn-off properly.

There are parasitic inductors in series with SRs, and the parasitic inductors lead to SR turn-off too early [4]. To solve this problem and improve the efficiency of the converter, some approaches are proposed in [4]-[8]. In [4], [6], some compensators are proposed across the SRs, and SRs can be driven properly with almost no body diode conduction. However, in these compensators, drain-source on resistance (R_{DS}(on)) is considered as constant. Thus, the compensation network are not precise when R_{DS}(on) is unfixed. In [9]-[16], digital detecting method for SRs are proposed. The effect of R_{DS}(on) can be eliminated and SRs can be turned on with no body diode conduction by digital detecting method.

There are many literatures about optimal turn-off time, but few literatures about turn-on time. In compensators or digital detecting method, SRs are turned on by detecting turn-on of body diodes of SRs. However, there are always ringing voltage across SRs at high load current when the current flowing through SRs decreases to zero. When minimum of ringing voltage reaches close to zero, the body diodes of SRs become turned on. This causes early turn-on of the SRs and causes abnormal operation.

In this paper, the LLC dc-dc converter with the filter circuit for SR driver circuit is proposed. By using the filter for SR driver circuit, LLC dc-dc converter can work well and keep high efficiency at high load current. A 1.26kW experimental prototype had been built and tested to verify the operating principle. The remaining of this paper is arranged as follows. The analysis of the voltage across SRs is presented in Section II. The experimental verification is shown in Section III. The conclusion of the paper is given in Section IV.

II. ANALYSIS OF THE VOLTAGE ACROSS SRS

For high load current applications, the conduction loss of secondary switches is proportional to the square of load current in synchronous rectification LLC dc-dc converter. Therefore, two transformers with serious-input and parallel-output are adopted to reduce current stress of transformer secondary switches, which is shown in Fig. 1. Because the two transformers primary are in series, the current flowing through the two transformers are the same, and the load current is divided by the two transformers and synchronous rectifiers.

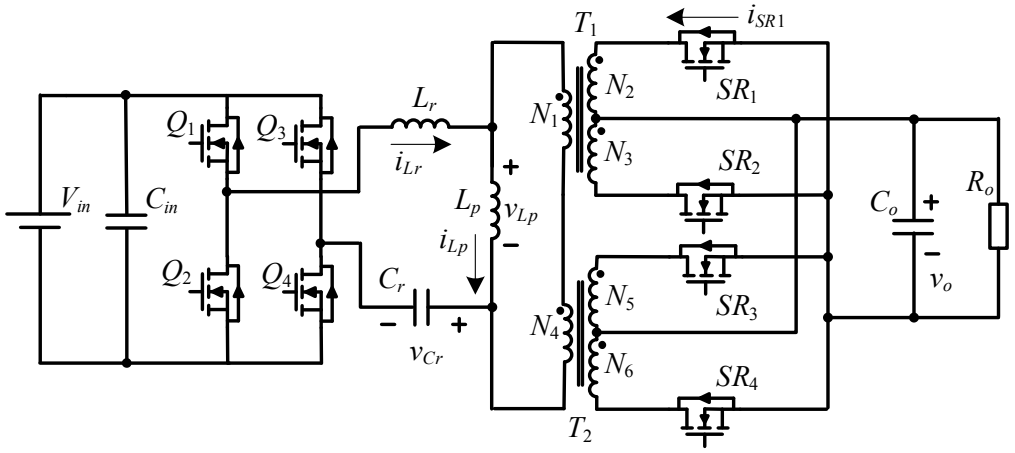


Fig. 1. LLC dc-dc converter for high load current application.

To simplify the analysis of the LLC dc-dc converter, some assumptions are adopted:

1) All active switches are ideal except their body diode and output capacitances. The output capacitances of switches Q_1-Q_4 are the same, i.e. $C_{oss,Q1}=C_{oss,Q2}=C_{oss,Q3}=C_{oss,Q4}$, and the output capacitances of switches SR_1-SR_2 are the same, i.e. $C_{oss,SR1}=C_{oss,SR2}=C_{oss,SR3}=C_{oss,SR4}$.

2) High frequency transformer is modeled by a large magnetizing inductance and small leakage inductance, an ideal transformer with turns-ratio n:1:1=N_1: N_2: N_3 = N_4: N_5: N_6.

3) If the dead time of primary side inverter is neglected, the driving signals of switches Q_1, Q_4 and switches Q_2, Q_3 are complementary with constant duty cycle 0.5.

4) During t_0~t_2 and t_3~t_5, the rectifier's current is approximated to a sinusoidal pulse.

Fig. 2 shows the key waveforms of the LLC dc-dc converter with SRs.

As shown in Fig. 2, at high load current, there is severe voltage ringing across SRs when series resonant current i_{Lr} decreases to parallel resonant current i_{Lp}. In SR LLC dc-dc converter, the turn-on time is usually detected by the voltage v_{DS} of SRs. The forward voltage drop of body diodes $-V_F$ of SRs are detected to create turn-on time for SRs, and when the current flowing through source to drain of SRs decreases to zero, the SRs are turned off. Thus, if the voltage ringing is large, it would cause the SRs to turn-on too early and make the circuit work abnormally.

To solve the problem of turn-on early of SRs, the voltage vds across SRs is analyzed as bellow.

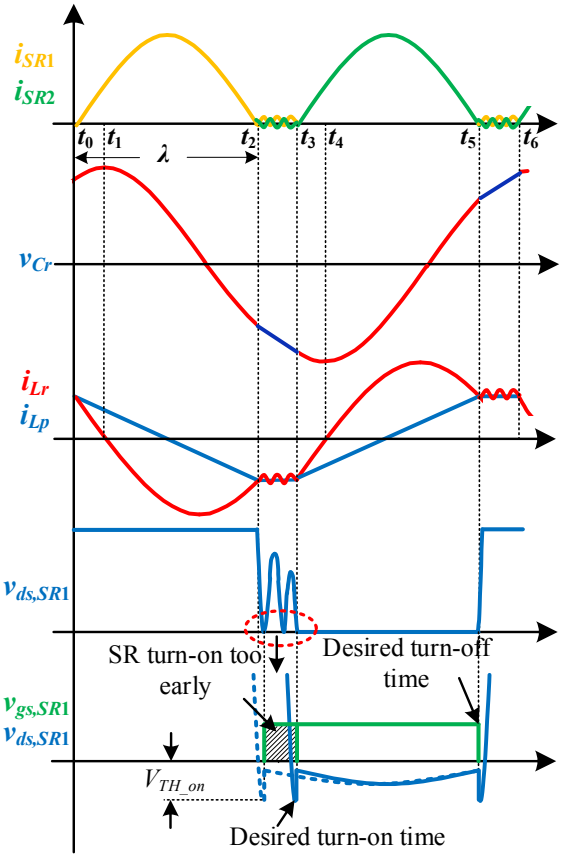


Fig. 2. Key waveforms.

For LLC dc-dc converter, the peak current flowing through source to drain of SR is

$$I_{SR,peak} = I_{SR1,peak} = \frac{\pi I_o T_s}{8\lambda} = \frac{\pi V_o}{8\lambda f_s R_o}. \quad (1)$$

where λ is time interval during t_0 to t_2, f_s is switching frequency, V_o is output voltage, I_o is load current and R_o is load resistor.

As shown in Fig. 2, the current i_{SR1} satisfies

$$i_{SR}(t-t_0)=\begin{cases} I_{SR,peak}\sin[\frac{1}{2f_s\lambda}\omega_s(t-t_0)], & 0<t<t_2 \\ 0, & t_2<t<t_3 \end{cases}. \quad (2)$$

where ω_s is switching angle frequency.

The peak current of i_{Lp} is

$$I_{Lp,peak}=\frac{nV_o\lambda}{L_p}. \quad (3)$$

Thus, during t_0~t_2, the current i_{Lp} satisfies

$$i_{Lp}(t-t_0)=\frac{nV_o\lambda}{L_p}-\frac{2nV_o}{L_p}(t-t_0). \quad (4)$$

To simplify the analysis, λ is approximated as

$$\lambda=\frac{f_s}{f_r}\cdot\frac{T_s}{2}=\frac{\pi}{\omega_{r1}}. \quad (5)$$

where ω_1 is

$$\omega_{r1}=\sqrt{\frac{1}{L_rC_r}}. \quad (6)$$

During t_1~t_2, resonant capacitor C_r is discharged by current i_{Lr}, and the voltage across resonant capacitor C_r is decreased, it has

$$v_{Cr}(t-t_1)=\frac{C_rV_{Cr,peak}+\int_{t_1}^{t}i_{Lr}(t-t_1)dt}{C_r}. \quad (7)$$

The current i_{Lr} satisfies

$$i_{Lr}(t-t_0)=i_{Lp}(t-t_0)-\frac{i_{SR}(t-t_0)}{n}. \quad (8)$$

During t_1~t_4, the current i_{Lr} can be approximated as

$$i_{Lr}(t-t_1)=-i_{Lr,\max}\sin(\omega_st). \quad (9)$$

And $V_{Cr,peak}$ is

$$V_{Cr,peak}=\frac{\int_0^{T/2}i_{Lr,\max}\sin(\omega_st)dt}{2C_r}=\frac{i_{Lr,\max}}{\omega_sC_r}. \quad (10)$$

According to equations (2), (4) and (8), to get $i_{Lr,max}$, when

$$\frac{di_{Lr}(t_x)}{dt}=-\frac{2nV_o}{L_p}-\omega_sI_{SR,peak}\cos[\frac{1}{2f_s\lambda}\omega_s(t_x-t_0)]=0, \quad (11)$$

and t_x is

$$t_x=\frac{2f_s\lambda}{\omega_s}\arccos(\frac{2nV_o}{-\omega_sI_{SR,peak}L_p})+t_0 \quad (12)$$

Substitute (2)-(5) and (12) to (8), $i_{Lr,max}$ is

$$\begin{aligned} i_{Lr,\max}&=-i_{Lr}(t_x-t_0)=-i_{Lp}(t_x-t_0)+\frac{i_{SR}(t_x-t_0)}{n} \\ &=-\frac{n\pi V_o}{\omega_{r1}L_p}+\frac{2nV_o}{\omega_{r1}L_p}\arccos(\frac{8nR_o}{-\pi L_p\omega_{r1}}) \\ &+\frac{\omega_{r1}\pi V_o}{4n\omega_sR_o}\sin[\arccos(\frac{8nR_o}{-\pi L_p\omega_{r1}})]. \end{aligned} \quad (13)$$

As at t_1, the current i_{Lr} is zero, it has

$$i_{Lp}(t_1-t_0)-\frac{i_{SR}(t_1-t_0)}{n}=0. \quad (14)$$

Substitute (2)-(5) to (8), the time interval t_0~t_1 satisfies

$$f(t_1-t_0)=\frac{n\pi V_o}{\omega_{r1}L_p}-\frac{2nV_o}{L_p}(t_1-t_0)-\frac{\pi V_o\omega_{r1}}{4n\omega_sR_o}\sin[\omega_{r1}(t_1-t_0)]=0. \quad (15)$$

Thus, the time interval t_1~t_2 is

$$t_2-t_1=\lambda-(t_1-t_0). \quad (16)$$

Substitute (9)-(10) and (13) to (7), the voltage $v_{Cr}(t_2)$ can be got.

During t_2~t_3, as inductance L_p is much larger than L_r, the current i_{Lr} can be regarded as equaling to i_{Lp}. At time t_2, it has

$$i_{Lr}(t-t_2)=i_{Lp}(t-t_2)=\frac{2nV_o}{L_p}\cdot\frac{\pi}{2\omega_{r1}}=\frac{n\pi V_o}{\omega_{r1}L_p}. \quad (17)$$

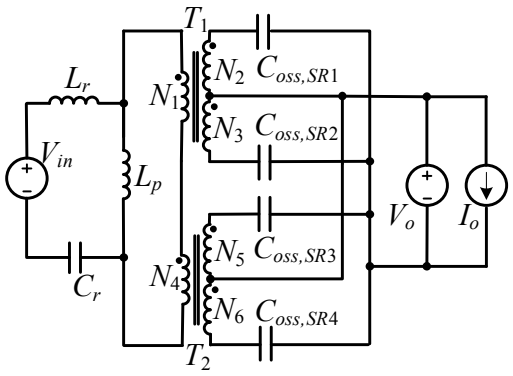
The voltage across transformer primary is

$$v_{Lp}(t_2)=\frac{L_p}{L_p+L_r}[V_{in}-v_{Cr}(t_2)]. \quad (18)$$

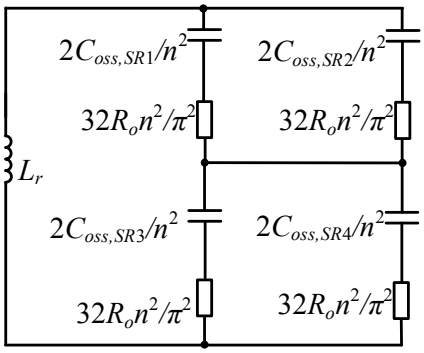
Thus $v_{ds,SR1}(t_2)$ is

$$\begin{aligned} v_{ds,SR1}(t_2)&=V_o+\frac{v_{Lp}(t_2)}{2n} \\ &=V_o+\frac{L_p[V_{in}-v_{Cr}(t_2)]}{2n(L_p+L_r)}. \end{aligned} \quad (19)$$

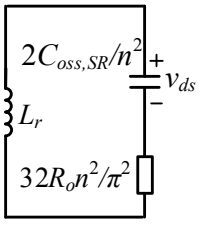
During t_2~t_3, parasitic capacitor C_{oss} of SRs are resonant with inductor L_r. During the voltage ringing, transformer primary switches are conducting, and transformer secondary switches are turned off. The parasitic capacitor of switches C_{oss} is in series with the circuit. The equivalent circuit is shown in Fig. 3(a).



(a) Equivalent circuit during voltage ringing



(b) Simplified equivalent circuit



(c) Equivalent RLC circuit

Fig. 3. Equivalent circuit.

Because $C_r >> C_{oss}$, $C_o >> C_{oss}$, and $i_{Lr}=i_{Lp}$ during t_2~t_3, the equivalent circuit in Fig. 3(a) can be simplify to the circuit as shown in Fig. 3(b), and the impedance is transferred into transformer primary. If the parasitic capacitors of SRs C_{oss} are the same, the resonant frequency of the RLC circuit is

$$f_{r2}=\frac{1}{2\pi\sqrt{L_r\frac{2C_{oss,SR}}{n^2}}}. \tag{20}$$

As shown in Fig. 3(c), the simplified equivalent circuit can be regarded as a second-order network. If the voltage across capacitor u_c is selected as state variables, according to KVL, there is

$$L_r\frac{2C_{oss,SR}}{n^2}\frac{d^2v_{ds,R1}}{dt^2}+\frac{64R_oC_{oss,SR}}{\pi^2}\frac{dv_{ds,R1}}{dt}+v_{ds,R1}=0. \tag{21}$$

Characteristic equation is

$$LCp^2+RCp+1=0. \tag{22}$$

It can be obtained as

$$\begin{aligned}p_{1,2}&=-\frac{R}{2L}\pm\sqrt{(\frac{R}{2L})^2-\frac{1}{LC}}\\&=-\frac{16R_on^2}{\pi^2L_r}\pm\sqrt{(\frac{16R_on^2}{\pi^2L_r})^2-\frac{n^2}{2L_rC_{oss,SR}}}.\end{aligned} \tag{23}$$

Because the real of (23) is less than zero, and $\frac{R}{2}\sqrt{\frac{C}{L}}<1$ is always satisfied, the RLC circuit operates at underdamped The initial value of the voltage across parasitic capacitor $v_{coss,SR1}$ and the current flowing through inductor i_L are

$$v_{Coss,SR1}(t_{2+})=v_{Coss,SR1}(t_{2-})=v_{ds,SR1}(t_2) \tag{24}$$

And
$$i_{Lr}(0_+)=i_{Lr}(0_-)=0. \tag{25}$$

Setting

$$\alpha=\frac{R}{2L},\ \omega_0=\sqrt{\frac{1}{LC}},\ \omega=\sqrt{\frac{1}{LC}-(\frac{R}{2L})^2}=\sqrt{\omega_0^2-\alpha^2}. \tag{26}$$

Thus, p_1 and p_2 are

$$p_1=-\omega_0e^{-j\beta},\ p_2=-\omega_0e^{j\beta}. \tag{27}$$

β is

$$\beta=\arctan(\frac{\omega}{\alpha}). \tag{28}$$

The voltage across parasitic capacitor of SR_1 $v_{ds,SR1}$ is

$$v_{Coss,SR1}(t-t_2)=\frac{v_{Coss,SR1}(t_2)\omega_0}{\omega}e^{-\alpha t}\sin[\omega(t-t_2)+\beta]. \tag{29}$$

As the RLC circuit operates at underdamped, thus there is voltage ringing across SRs. And according to (29), when the voltage across parasitic capacitor of SR is less than zero, the SRs are turned on early. In order to solve this problem, the RC filter is paralleled with parasitic capacitors of SRs *Coss*, as shown in Fig. 4. The voltage across the filter capacitor satisfy

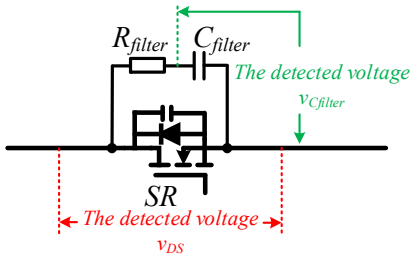


Fig. 4. The proposed filter circuits.

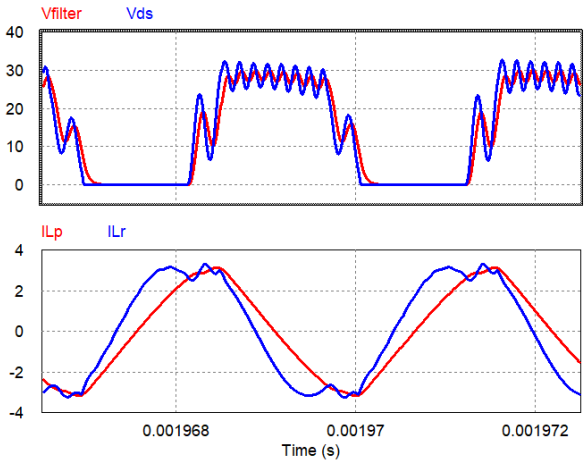
$$\begin{aligned}&v_{Coss,SR1}(t-t_2)-C_{filter}R_{filter}\frac{dv_{C,filter}(t-t_2)}{dt}\\&-\frac{v_{Coss,SR1}(t-t_2)-v_{C,filter}(t-t_2)}{R_{filter}}=0.\end{aligned} \tag{30}$$

The voltage $v_{C,filter}(t-t_2)$ is

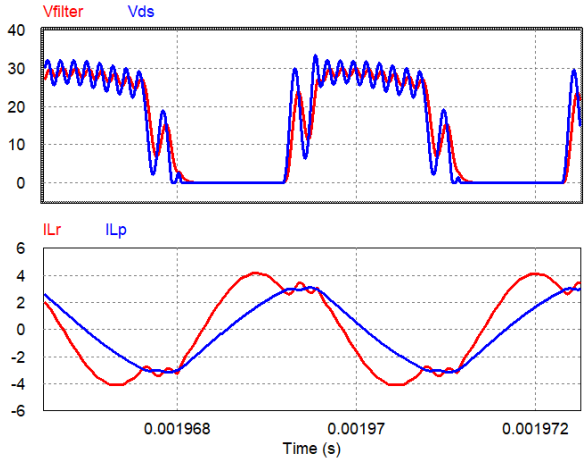
$$v_{C,filter}(t-t_2) = Ce^{\int \frac{1}{R_{filter}{}^2 C_{filter}} dt}$$

$$+e^{\int \frac{1}{R_{filter}{}^2 C_{filter}} dt} \int v_{\mathrm{Coss,SR1}}(t-t_2) \frac{[1-\frac{1}{R_{filter}}]}{C_{filter} R_{filter}} e^{\int -\frac{1}{R_{filter}{}^2 C_{filter}} dt} dt. \quad (31)$$

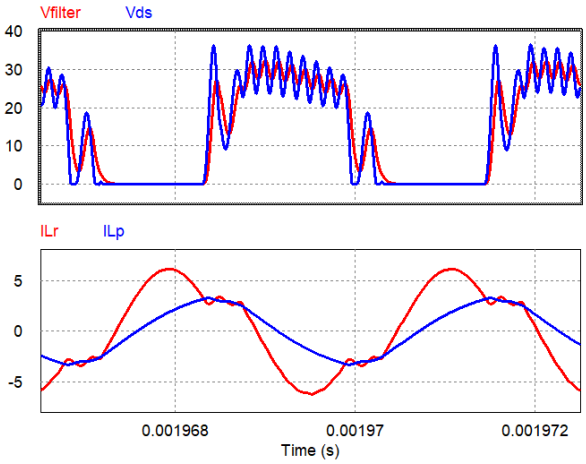
It can be seen from (31), The voltage $v_{C,filter}(t-t_2)$ can be expressed by the voltage across parasitic capacitor of SR $v_{\mathrm{Coss,SR1}}(t-t_2)$. As shown in Fig. 4, if the voltage across the filter capacitor is detected to create turn-on signal for SRs, the minimum of detected voltage less than zero problem can be solved by adjust the filter parameter C_{filter} and R_{filter}.



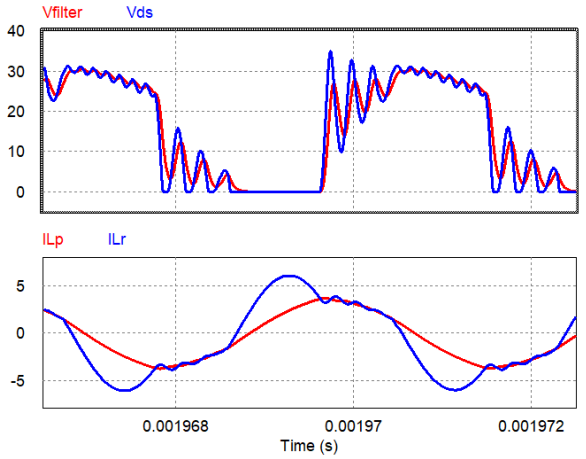
(a) 380V input 14V output and 40A load current



(b) 380V input 14V output and 60A load current



(c) 380V input 14V output and 90A load current



(d) 250V input 14V output and 60A load current

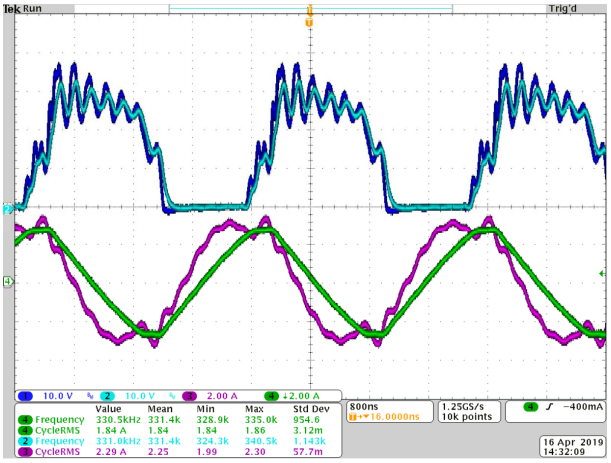
Fig. 5. Simulation waveforms of the voltage v_{ds} across SRs at different input voltage and load current condition

Fig. 5 shows the simulation waveforms of the voltage across SRs at different input voltage and load current condition. As we can see that if load current is high, the voltage across SR is prone to decrease to zero when the current flowing through secondary switches are zero. By using the proposed RC filter, the voltage across capacitor in the filter is always higher than zero. Therefore, the problem of turn-on time early can be solved by sensing the voltage across the capacitor in the filter instead of sensing the voltage across drain to source of the SRs.

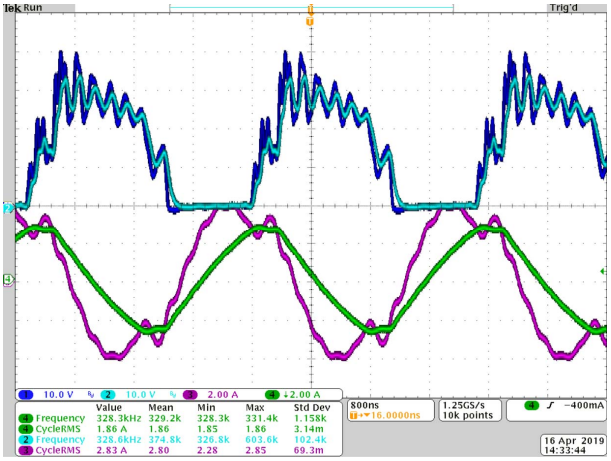
III. Experimental Verification

To verify the analysis, a 250V~430V input, 14V output, 1.26kW prototype is designed and tested at two different input voltages 250V and 380 V. As shown in Fig. 1, the LLC dc-dc converter can operate at 90A high load current well by using the filter circuit in Fig. 4.

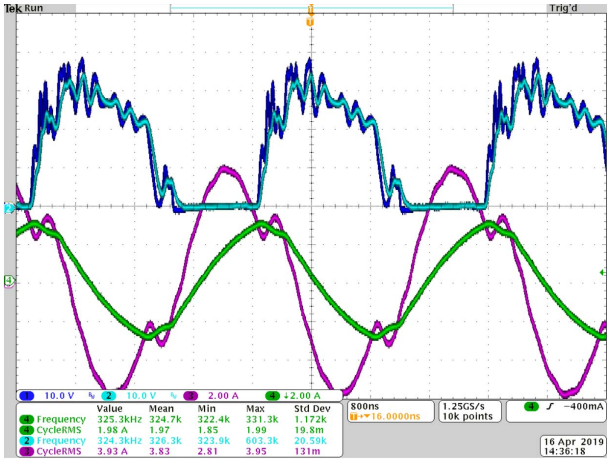
The key waveforms are shown as bellow,



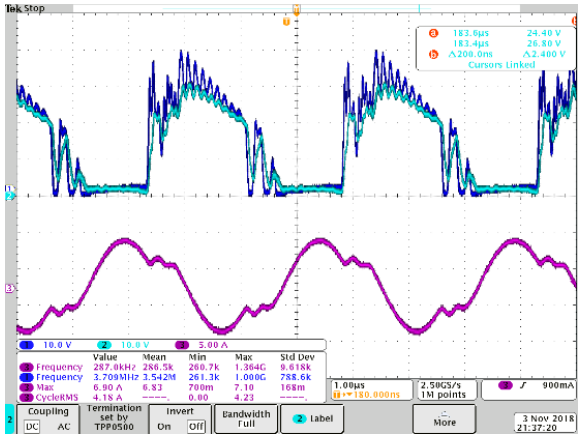
(a) 380V input 14V output and 40A load current



(b) 380V input 14V output and 60A load current



(c) 380V input 14V output and 90A load current



(d) 250V input 14V output and 60A load current

Fig. 6. Waveforms of the voltage v_{ds} across SRs at different input voltage and load current condition

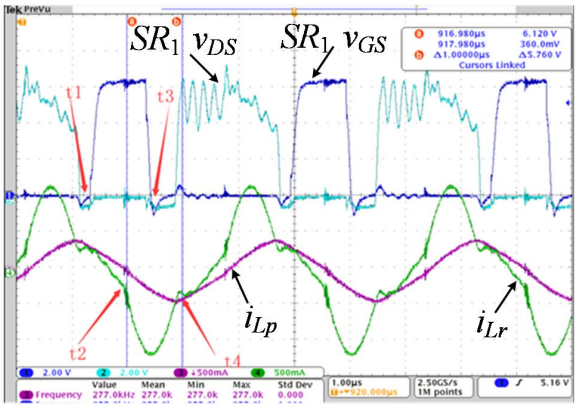
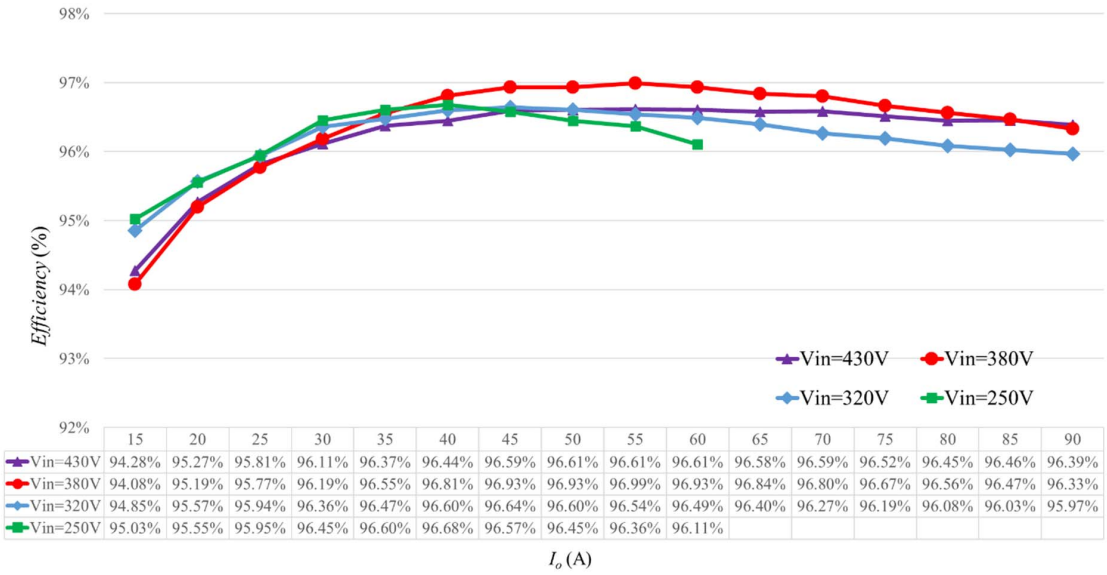


Fig. 7. Waveforms of the voltage v_{ds} across SRs when SRs are turned on early

As shown in Fig. 6(a)-(c), he dark blue line represents the voltage across SRs and the light blue line represents the voltage across the filter capacitor. When load current is high at the same input voltage, the voltage v_{ds} across SRs is prone to zero before the SRs are turned on. From Fig. 6 (b) and (d), when load current are the same, the voltage v_{ds} across SRs is prone to zero with lower input voltage.

In Fig. 7, If voltage v_{ds} across SR is detected to generate turn-on signal for SR, SR is turned on early at time t_1, and the circuit operates abnormally. If the voltage across the capacitor in the filter is sensed to generate turn-on signal for SRs, the problem of turn-on early of SRs is solved and the load current can be higher.

Fig. 8 shows the measured efficiency of the proposed *LLC* dc-dc converter at 250V, 320V, 380V and 430V input. When the input voltage is 320V, 380V and 430V, the full load current is 90A, when the input voltage is 250V, the full load current is 60A. Peak efficiency of the circuit is 96.99% at 55A load current when input voltage is 380V and output voltage is 14V.



	15	20	25	30	35	40	45	50	55	60	65	70	75	80	85	90
Vin=430V	94.28%	95.27%	95.81%	96.11%	96.37%	96.44%	96.59%	96.61%	96.61%	96.61%	96.58%	96.59%	96.52%	96.45%	96.46%	96.39%
Vin=380V	94.08%	95.19%	95.77%	96.19%	96.55%	96.81%	96.93%	96.93%	96.99%	96.93%	96.84%	96.80%	96.67%	96.56%	96.47%	96.33%
Vin=320V	94.85%	95.57%	95.94%	96.36%	96.47%	96.60%	96.64%	96.60%	96.54%	96.49%	96.40%	96.27%	96.19%	96.08%	96.03%	95.97%
Vin=250V	95.03%	95.55%	95.95%	96.45%	96.60%	96.68%	96.57%	96.45%	96.36%	96.11%						

I_o (A)

Fig. 8. Measured efficiency

IV. Conclusion

This paper presents a zero-crossing filter for driving synchronous rectifiers of LLC dc-dc converters to eliminate the effect of voltage ringing across SRs for high load current applications. In the proposed LLC dc-dc converter, ZVS turn-on of the primary switches and secondary SRs is achieved, ZCS turn-off of secondary SRs is also realized. By detecting the voltage across the filter capacitor to create the turn-on signal for SRs, the problem of early SR turn-on is eliminated. In the proposed LLC dc-dc converter, wide input and output voltage ranges and high efficiency are realized.

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